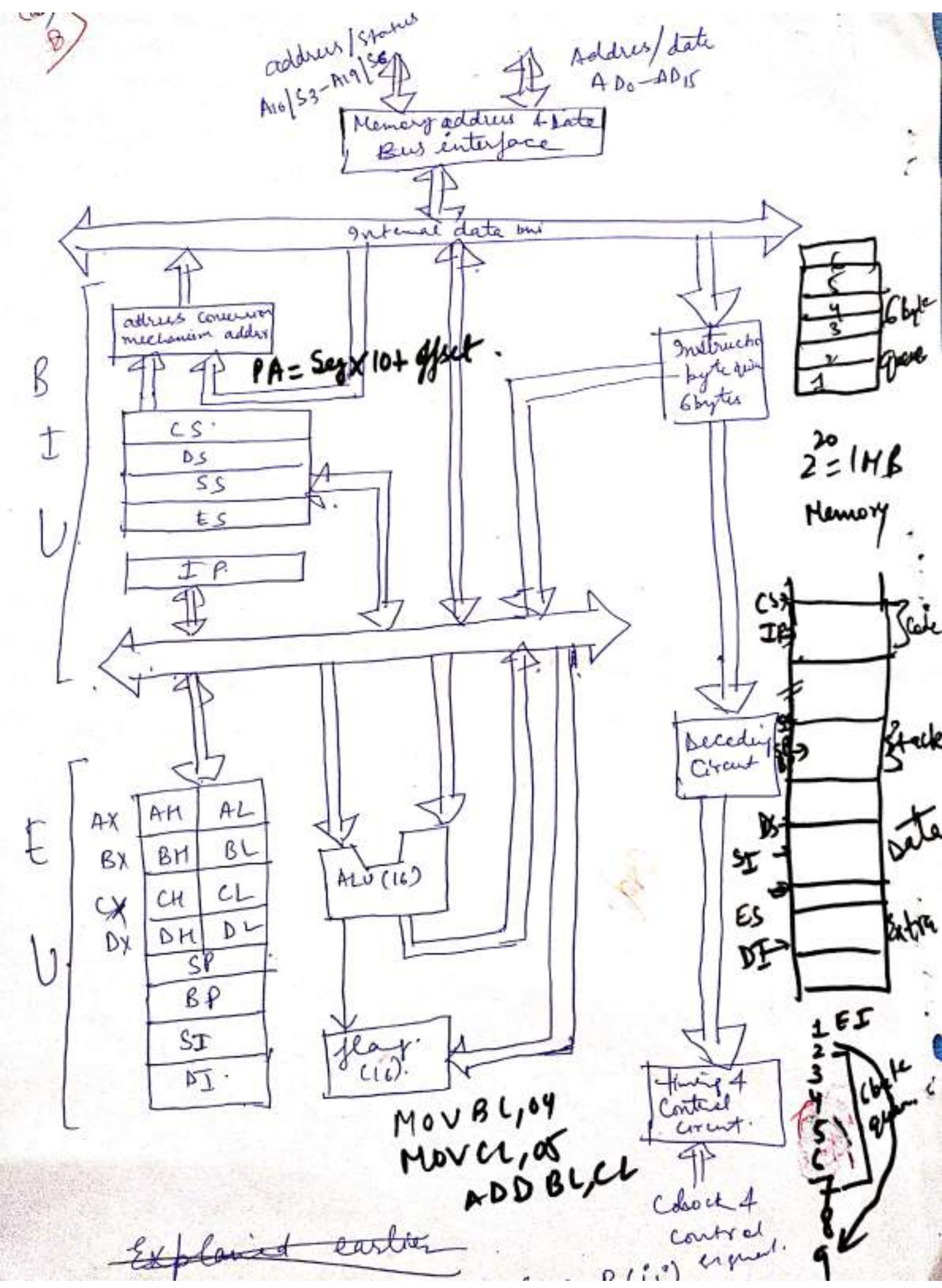

The Complete architecure of 8086 can be divided into the two parts a) Bus interface unit (BIU) & b) Execution unit (EU).

a) BIU → The bus interface unit contains the circuit for physical address calculation & predecoding instruction byte queue (6 bytes long). The BIU consists of 6 bytes long instruction register called queue & four stack Segment registers (ES, CS, SS, DS), one instruction pointer(IP) & an adder circuit to calculate the 20 bit physical addres of a location. This Bus interface unit will perform all extrd bus operations. they are fetching the instructions from memory, read / write data from / into memory or both and also supporting the instruction queue etc. The BIU fetches upto six instruction Bytes from memory & store these prefetched bytes in a FIFO register set called queue. when the execution unit is ready for execution of the instruction instead of fetching the byte from the memory, it reads a data byte from queue. The instructions from queue are taken for decoding sequentially. once a byte is decode. the queue is rearranged by pushing it out & the queue status is checked for the possibility of next opcode fetch cycle.

EU while the opcode is fetched by BIU, the EU executes the previously decoded instruction. Concurrently. The BIU along with EU thus perform a pipeline. The EU contain the register set of 8086 except segment register & IP. It has 16 bit ALU able to perform arithmetic & logic operations. The 16 bit flag register reflects the

result of execution by the ALU. The decoding unit decodes the opcode bytes issued from the instruction byte queue. The timing & Control unit derives the necessary control signals to execute the instruction opcode received from the queue, depending up on the information made available by the decoding circuit. The execution unit may pass the results to the bus interface unit for storing them in memory.